A New Calculation Approach of Transistor Noise Parameters as a Function of Gatewidth and Bias Current

Ahmed Gasmi, Bernard Huyart, *Member, IEEE*, Eric Bergeault, and Louis P. Jallet

***Abstract*— In this paper a new method to calculate the noise parameters of transistors T_i (MESFET or HEMT) as a function of gatewidth and drain–bias current is presented. This method needs the knowledge of the R, P, and C coefficients. It is based on the measurement of the noise parameters of a reference transistor T_r at two bias points ($I_{\rm ds1}$ and $I_{\rm ds2}$), and the equivalent circuit elements' values of all transistors T_i. Using this method, the noise parameters ($F_{\rm min}$, $\Gamma_{\rm opt}$, R_n) for two MESFET's T_i biased at another current $I_{\rm ds3}$ are obtained. Good agreement between the predicted and measured noise parameters' values is obtained for a broad frequency range (4–20 GHz).**

***Index Terms*—HEMT, MESFET, MMIC, modelization, noise.**

I. Introduction

ACTIVE circulator design has been enhanced considerably thanks to microwave monolithic integrated circuits (MMIC's) technology [1]. A design difficulty is to reach a compromise between the isolation, insertion loss, and return loss of a passive circulator and the noise of an active circulator. Thus, it is necessary to be able to evaluate the noise figure of a circuit constituted of different transistors sizes with different drain current values. A partial study of this problem has been made in [2]. In [2] semi-empirical relationships for the noise parameters ($F_{\rm min}$, R_n, $Z_{\rm opt}$) as a function of the gatewidth under a zero gate-bias condition is suggested. These expressions cannot be used at another bias current because it is necessary to modify the fitting factors $K1$, $K2$, $K3$, and $K4$ of (2)–(5) in [2]. A noise model for the same problem has been done in [3]. This model is similar to the one experimentally used in [4] and [5]. In the case of [3], the noise parameters ($F_{\rm min}$ and R_n) of FET transistors depending on the bias current are given. On the other hand, no result has been presented to check the validity of the current dependence for the optimum source admittance. In this model, the noise parameters of the transistor has been calculated with two uncorrelated noise sources at the gate and the drain. In this case, the used MESFET's have a strong correlation between the two noise sources, and, therefore, it is not possible to use the noise model of [3] (see Section IV). Another solution to this problem has been given by [6] where a noise equivalent circuit of an intrinsic transistor (HEMT, MESFET) is represented by a noiseless model with two noise sources, i.e., a voltage one (e_h) at the input and a current one (i_h) at the output. The noise parameters are then calculated taking into account that these noise sources are independent [6]. The mean square values of the noise sources e_h and i_h are, respectively, proportional to the two equivalent temperatures T_g and T_d of the gate–source and drain-source resistances ($r_{\rm gs}$ and $r_{\rm ds}$) of the transistor. Moreover, experience shows that the temperature T_g is weakly sensitive to the bias current $I_{\rm ds}$ and is virtually equal to the room temperature [7], [8]. On the other hand, T_d is a very strong function of the drain–bias current ($I_{\rm ds}$). Indeed, [7] and [8] have shown that the product of conductance $g_{\rm ds}$ ($1/r_{\rm ds}$) and temperature T_d is proportional to the drain–bias current. Therefore, knowledge of the temperature T_d at one bias point allows the determination of the proportional coefficient between $g_{\rm ds}T_d$ and $I_{\rm ds}$. Then, from the equivalent circuit of the transistor, one can calculate its noise parameters at another bias point taking into account that the other transistor resistances are at the physical temperature T_a of the chip. However, this representation is only valid where the condition $1 \leq 4NT_0/T_{\rm min} < 2$ is verified for the intrinsic transistor model; N is its noise parameter equal to $g_n R_{\rm opt}$ [6], $T_{\rm min}$ is its minimum noise temperature, and T_0 is the standard temperature of 290 K. But, the right-hand side (RHS) of this condition is not always verified depending on the technological parameters.

An analytical solution has been derived by [13] and [14]. This method permits us to determine the transistor noise parameters from foundry technological parameters such as carrier concentration, epi-layer thickness, low field mobility, etc. The difficulty is then to know precisely these technological data. Moreover, verification of the theoretical value by measurement has only been done for the minimum noise figure $F_{\rm min}$ for the low-noise operating conditions of the transistors [14].

In this paper, the authors propose a method to calculate the noise parameters of transistors of the same technology as a function of gatewidth and drain–bias current. This method is based on the Van der Ziel model [10], [11], [15], [16]. Noise contributions of the ohmic resistances r_g, r_d, and r_s are determined by the physical temperature T_a of the chip. The authors suppose that the noise–current sources of the intrinsic transistor are correlated. These sources are described by the noise coefficients P, R, and C' [9]–[11]; C' is the correlation coefficient, P and R are the noise parameters depending upon the technological parameters and biasing conditions [14].

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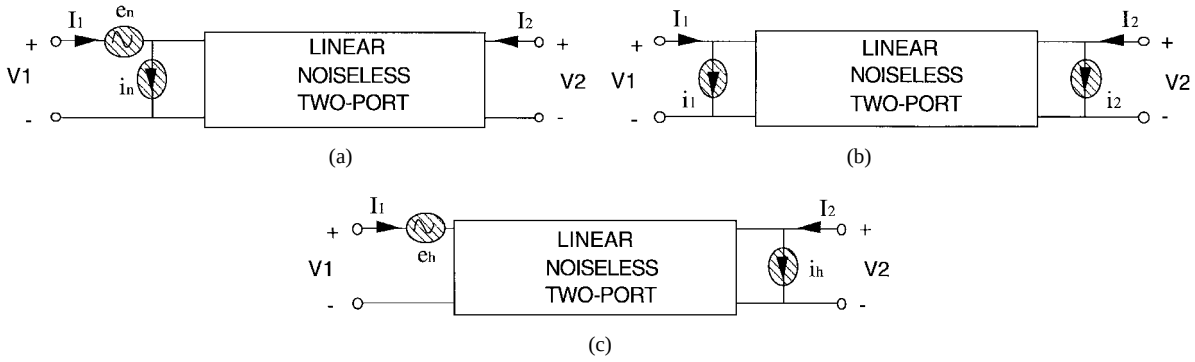


Fig. 1. Noise representation in linear two-ports: (a) involving current and voltage noise sources at the input, (b) involving current noise sources at the input and output, and (c) involving voltage noise source at the input and current noise source at the output.

In Section II, the authors describe how to determine these parameters from:

- equivalent circuit element values as a function of gatewidth and drain–bias current;
- noise coefficients P and C' of the intrinsic model of a single transistor at two different bias points and the noise coefficient R at a single bias point.

The main originality of the authors' method is to approximate the P, C' curves given in [14] by analytical functions and to calculate the coefficients of these functions from the measurements of noise parameters. Then, in Section III, the authors compare the experimental results with those obtained by this method.

II. Determination of the Noise Coefficients R, P, C' as a Function of Gatewidth (Z) and Bias Current ($I_{\rm ds}$)

A. Extraction of Noise Sources for a Noisy Two-Port

Fig. 1 shows the different representations of a linear noisy two-port, characterized by its $[Y]$ admittance matrix and its noise parameters ($F_{\rm min}$, $Y_{\rm opt}$, R_n). $F_{\rm min}$ is the minimum noise figure, $Y_{\rm opt}$ is the optimum source admittance required to have $F_{\rm min}$, and R_n is the equivalent noise resistance. It has been shown in [12], that the mean square value of the noise sources i_1, i_2, and e_h are given by

$$\langle|i_1|^2\rangle = 4KT_0B(G_n + R_n|Y_{11} - Y_c|^2) \quad (1)$$

$$\langle|i_2|^2\rangle = 4KT_0BR_n|Y_{21}|^2 \quad (2)$$

$$\langle|e_h|^2\rangle = \frac{4KT_0B(G_n + R_n|Y_{11} - Y_c|^2)}{|Y_{11}|^2}. \quad (3)$$

The noise current sources i_1 and i_2 are not independent. These sources are linked by the correlation coefficient C' defined by the relation:

$$C' = \frac{\langle i_1 i_2^*\rangle}{\sqrt{\langle|i_1|^2\rangle\langle|i_2|^2\rangle}} = \frac{Y_{21}^*(Y_{11} - Y_c)}{|Y_{21}|\sqrt{\dfrac{G_n}{R_n} + |Y_{11} - Y_c|^2}} \quad (4)$$

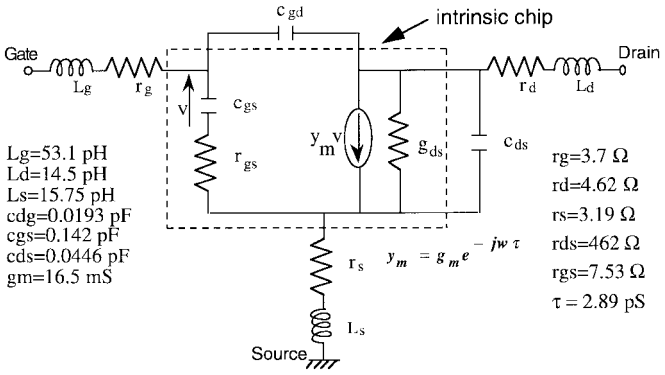


Fig. 2. Small signal equivalent circuit of the MESFET. The elements values are given for a transistor of $0.5 \times 200\,\mu{\rm m}^2$ gate dimensions and biased at $I_{\rm ds} = I_{\rm dss}/5$ and $V_{\rm ds} = 5$ V.

where Y_{ij} are the $[Y]$ admittance matrix elements and Y_c is the correlation admittance between e_n and i_n [see Fig. 1(a)],

$$Y_c = \frac{\langle i_n e_n^*\rangle}{\langle|e_n|^2\rangle} = \frac{F_{\rm min} - 1}{2R_n} - Y_{\rm opt}. \quad (5)$$

The equivalent noise conductance G_n can be expressed as

$$G_n = \frac{\langle|i_n - Y_c e_n|^2\rangle}{4KT_0B} = (F_{\rm min} - 1)\left(G_{\rm opt} - \frac{F_{\rm min} - 1}{4R_n}\right) \quad (6)$$

where K is the Boltzman constant, T_o is the standard reference temperature equal to 290 K, and B is the frequency bandwidth. The brackets "$\langle\rangle$" indicate time average and the asterisk denotes the complex conjugate. For the intrinsic zone of the transistor, this extraction method will be used to analyze the behavior of the noise sources and noise coefficients (R, P, and C') versus frequency for a given bias point.

B. Determination of the Noise Coefficient R

For the intrinsic model of the transistor (Fig. 2), the mean square value of the noise current i_1 in the gate–source path is related to a noise coefficient R [9]–[11] as follows:

$$\langle|i_1|^2\rangle = \frac{4KT_0BC_{\rm gs}^2\omega^2R}{g_m} \quad (7)$$

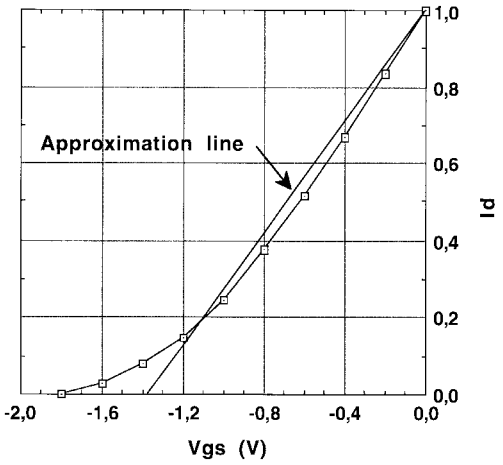


Fig. 3. DC current–voltage characteristics ($V_{\rm ds} = 5$ V) of the MESFET's employed in this paper.

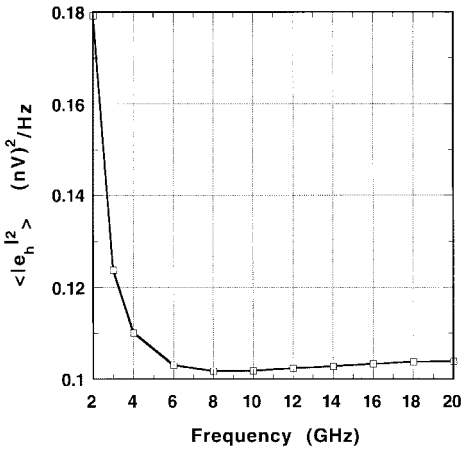


Fig. 4. Noise voltage source $\langle|e_h|^2\rangle$ of the intrinsic model of a $0.5 \times 200\,\mu$m^2 MESFET biased at $I_{\rm ds} = I_{\rm dss}/5$ and $V_{\rm ds} = 5$ V.

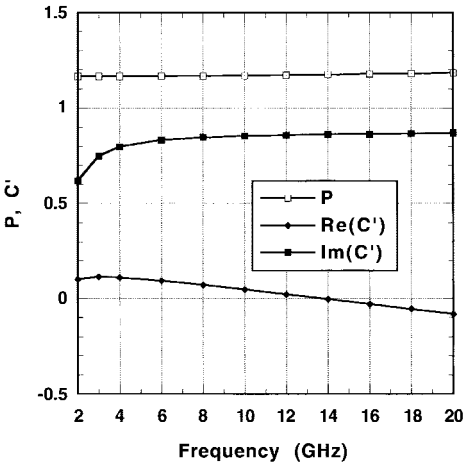


Fig. 5. Noise coefficients P and C' (versus frequency) of the intrinsic model of a $0.5 \times 200\,\mu$m^2 MESFET biased at $I_{\rm ds} = I_{\rm dss}/5$ and $V_{\rm ds} = 5$ V.

where $C_{\rm gs}$ is the gate–source capacitance, g_m is the transconductance of the transistor, and ω is the signal angular frequency at which will be calculated the transistor noise parameters. The mean square value of the noise voltage e_h is related to the noise temperature T_g for the resistance $r_{\rm gs}$ by the following [7], [8]:

$$\langle|e_h|^2\rangle = 4KT_g r_{\rm gs} B. \tag{8}$$

In this case, the authors haven't made any hypothesis on the value of the correlation factor of sources e_h and i_h because $r_{\rm gs}$ varies with the bias current $I_{\rm ds}$. The authors have then defined the equivalent noise source $\langle|e_h|^2\rangle$ for each $r_{\rm gs}$ which is always carried to a constant temperature T_g. This is proven in Section III. By combining (1), (3), (7), and (8) and defining $Y_{11} = j\omega C_{\rm gs}/1 + j\omega C_{\rm gs} r_{\rm gs}$ for the intrinsic model shown in Fig. 2, the noise coefficient R can be simply expressed as a function of the noise temperature T_g and the equivalent circuit elements

$$R = \frac{T_g}{T_0}\,\frac{g_m r_{\rm gs}}{1 + (r_{\rm gs}\omega C_{\rm gs})^2}. \tag{9}$$

The value of T_g is determined by identifying the noise voltage $\langle|e_h|^2\rangle$ given by (8) with the value obtained from (3) for an intrinsic chip.

C. Determination of the Noise Coefficient P

Following the theory developed in [13], the mean square value of the noise current i_2 (noise source between drain and source) depends simply on the small signal elements of the intrinsic transistor model, gatewidth Z, gate length L_g, and dc drain current $I_{\rm ds}$:

$$\langle|i_2|^2\rangle = 4KT_0 B\,\frac{g_{\rm ds}^2 + \omega^2 C_{\rm gd}^2}{g_{\rm ds}^2}\,\frac{g_m}{C_{\rm gs}}\,L_g(\alpha Z + \beta I_{\rm ds}). \tag{10}$$

$C_{\rm gd}$ is the gate–drain capacitance. The two fitting parameters α and β are fairly constant because they are independent of the active layer geometry (gate length and epi-layer thickness) and material properties (low field mobility and carrier concentration). For the simplified intrinsic model shown in Fig. 2, (10) becomes

$$\langle|i_2|^2\rangle = 4KT_0 B\,\frac{g_m}{C_{\rm gs}}\,L_g(\alpha Z + \beta I_{\rm ds}). \tag{11}$$

Following [10] and [11], the noise source $\langle|i_2|^2\rangle$ can be expressed as

$$\langle|i_2|^2\rangle = 4KT_0 B g_m P. \tag{12}$$

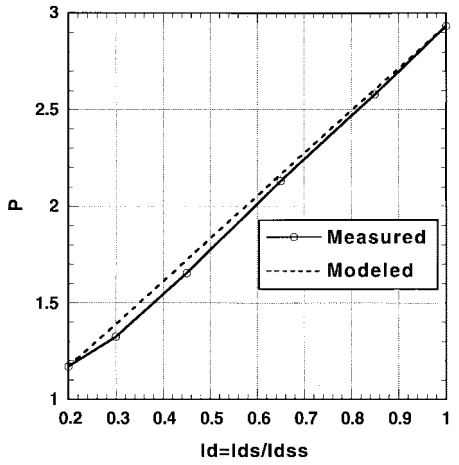
Identification of (11) and (12) shows that the noise coefficient P is a function of the geometrical size (L_g, Z), the capacitance $C_{\rm gs}$, and biasing conditions of the transistor

$$P = \frac{L_g(\alpha + \beta' I_d)}{\dfrac{C_{\rm gs}}{Z}} \tag{13}$$

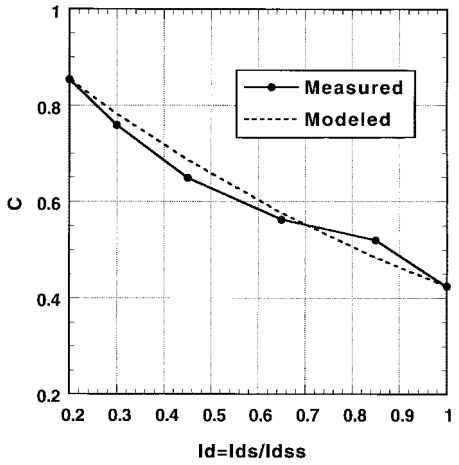
with $\beta' = \beta I_{\rm dss}/Z$ and $I_d = I_{\rm ds}/I_{\rm dss}$, where $I_{\rm dss}$ is the saturated drain current. On the other hand, the theoretical result given in [14, Fig. 6] shows that for a biasing current $I_{\rm ds}$ between $I_{\rm dsopt}$ (in the order of $0.1I_{\rm dss}$ to $0.2I_{\rm dss}$) and $I_{\rm dss}$, the noise coefficient P is linear with $V_{\rm gs}$, i.e.,

$$P = k + mV_{\rm gs} \tag{14}$$

where k and m are constants.



(a)



(b)

Fig. 6. (a) Comparison of measured and modeled coefficient P. (b) Comparison of measured and modeled coefficient C.

By using the static characteristic of the authors' MESFET's (Fig. 3), it can be seen that the percentage bias current I_d ($0.2 \leq I_d \leq 1$) is a quasi-linear function of the gate voltage $V_{\rm gs}$. Therefore, (14) becomes

$$P = A + BI_d. \tag{15}$$

In conclusion, (13) and (15) are consistent if P is independent of the gatewidth Z. This result was expected because the capacitance $C_{\rm gs}$ is proportional to Z. Moreover, the authors consider that $C_{\rm gs}$ is weakly dependent of I_d between $I_{\rm dsopt}$ and $I_{\rm dss}$. Equation (15) is verified experimentally in Section III. The constants A and B are determined from the knowledge of the noise coefficient P at two bias points. It should be noted that the noise coefficient P for these two bias points is obtained by substitution between (2) and (12). In this case, the mean square value of the noise current i_2 given by (2) is applied for the intrinsic transistor model shown in Fig. 2. This method is more precisely described in Section III.

D. Determination of the Noise Coefficient C'

From the intrinsic transistor model of Fig. 2 and for frequencies such that the $1/f$ noise is negligible, the complex correlation coefficient C' is imaginary and frequency-independent [9].

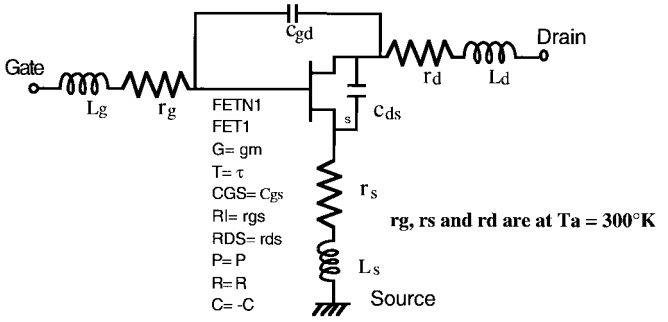


Fig. 7. Noise equivalent circuit of a transistor using the Van der Ziel model (Called FETN1 in LIBRA).

TABLE I
NOISE PARAMETERS OF A $0.5 \times 200\,\mu{\rm m}^2$ MESFET BIASED AT $I_{\rm ds} = I_{\rm dss}/5$ AND $V_{\rm ds} = 5$ V

Frequency (GHz)	Fmin (dB)	Mag(Γopt)	Ang(Γopt)	Rn/50
2	0.40	0.93	8.35	1.57
4	0.62	0.90	16.69	1.55
6	0.89	0.86	25.01	1.52
8	1.17	0.82	33.27	1.47
10	1.45	0.79	41.44	1.42
12	1.73	0.76	49.50	1.36
14	2.01	0.73	57.42	1.30
16	2.28	0.70	65.18	1.23
18	2.54	0.68	72.77	1.16
20	2.80	0.66	80.17	1.09

$$C' = jC \tag{16}$$

According to [13] and [14], this coefficient essentially depends on the gate length over epi-layer thickness ratio and is independent of the gatewidth Z. Similarly, it has been shown that in the saturated region, the noise coefficient C decreases as the drain–bias current increases. The correlation coefficient C is approximated by an analytical expression derived from the theoretical curve given in [14, Fig. 6] which will be verified experimentally in the next section

$$C = A' e^{-B' I_d}. \tag{17}$$

For transistors of the same technology, the constants A' and B' will only be determined by one transistor whose noise parameters and equivalent circuit elements are already known at two bias points. This calculation is described in the following section.

III. APPLICATION

Fig. 2 shows the small signal equivalent circuit for a MESFET of a MMIC foundry. This transistor has $0.5{\times}200\,\mu{\rm m}^2$ gate dimensions and is biased at $I_{\rm ds} = I_{\rm dss}/5$ and $V_{\rm ds} = 5$ V. The small signal equivalent circuit parameters are extracted from "hot–cold" on wafer S-parameters' measurements [17]. The noise parameters of this transistor in the 2–20 GHz frequency range are given in Table I. The noise parameters measurements are done on wafer with tuners. The authors have studied the influence of the transistor extrinsic elements (L_g, L_d, L_s, R_g, R_d, R_s, C_{dg}, $C_{\rm ds}$) [12] on the noise parameters

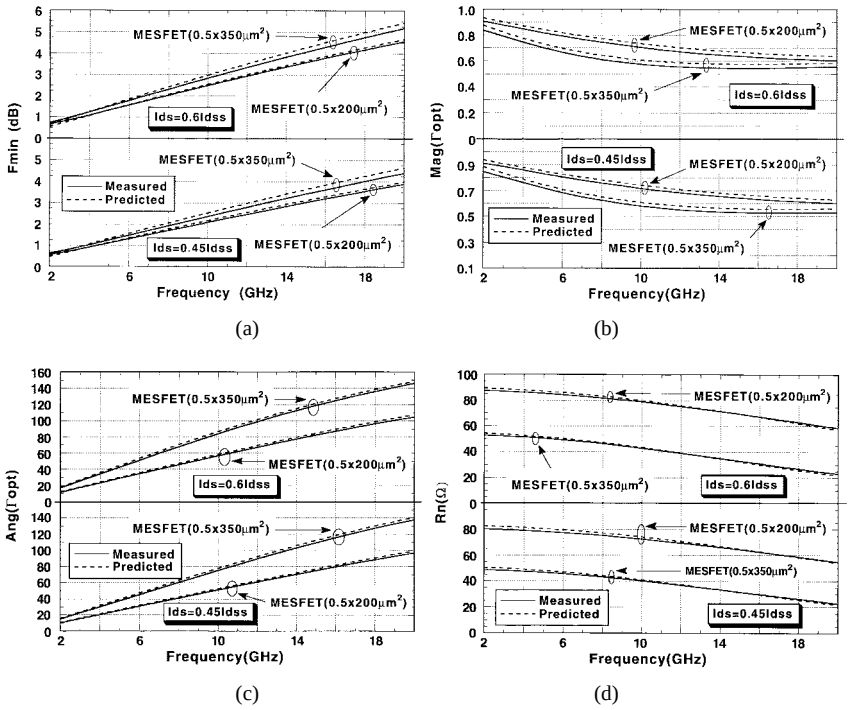


Fig. 8. Comparisons of measured and predicted noise parameters versus frequency for two MESFET's of different dimensions biased at $I_{\rm ds} = 0.6I_{\rm dss}$ and $I_{\rm ds} = 0.45I_{\rm dss}$ with $V_{\rm ds} = 5$V.

of the actual transistor using a commercial simulator (LIBRA) [15]. Taking into account these influences, the noise parameters of the intrinsic transistor (Fig. 2) can be obtained by de-embedding. The following is shown.

- In the 6–20-GHz frequency range, the noise voltage source $\langle|e_h|^2\rangle$ (3) of the intrinsic transistor model (Fig. 4) is nearly constant and equal to 0.104 $(\text{nV})^2$/Hz. This corresponds to a temperature T_g equal to 250 K for the resistance $r_{\rm gs}$. This result is not surprising because this depends on the precision with which the resistance $r_{\rm gs}$ is determined. Usually, noise parameters depend on the product $r_{\rm gs}T_g$ then, one can decrease the resistance $r_{\rm gs}$ to have $T_g = 300$ K. However, this is not useful for the noise parameters calculation [6, Sec. IV]. The substitution of this temperature value in (9), and the knowledge of the transistor equivalent circuit element values give the noise coefficient R. One notices that this coefficient may be determined at any operating bias since the temperature T_g is virtually independent of the bias current [7] and [8].
- The noise coefficient P of the intrinsic transistor model [see (2) and (12)] is invariant with the frequency (see Fig. 5) and equal to 1.17.
- The correlation coefficient C' [see (4)] between the noise current sources i_1 and i_2 of the intrinsic transistor model can be considered as imaginary (the real part decreases with frequency and is very small compared to the imaginary part) and slightly frequency dependent between 4–20 GHz (see Fig. 5). This result is in good agreement with [12]. Therefore, the authors have taken $C' = 0.85j$.

Knowing the noise parameters and equivalent circuit element values of the same transistor biased at $I_{\rm ds} = I_{\rm dss}$ and $V_{\rm ds} = 5$ V, the extraction of the noise coefficients P and C' with the above method has shown that these coefficients have the same variation as before. In the 4–20-GHz frequency band, these coefficients are equal to 2.93 and $0.42j$, respectively.

The coefficients A, B, A', B' of (15) and (17) are evaluated from the results obtained at $I_{\rm dss}/5$ and $I_{\rm dss}$; Therefore, the function of the noise coefficients P and C' versus bias current is known and is simply given by

$$P = 0.73 + 2.20\, I_d \tag{18}$$

$$C' = j\,1.02\, e^{-0.88\, I_d}. \tag{19}$$

These equations are verified (see Fig. 6) because a good agreement is obtained between measured and predicted parameters. It is necessary to remember that the transistor noise properties can be determined from the noise coefficients P, R, and C of the intrinsic model and the knowledge of its equivalent circuit elements. The authors can determine by simulation the noise parameters ($F_{\rm min}$, $\Gamma_{\rm opt}$, and R_n) of other transistors of the same technology at any drain–bias current between $I_{\rm dsopt}$ and $I_{\rm dss}$ by substituting the noise coefficients R, P, and C' given by (9), (18), and (19) in the noise-equivalent circuit of an intrinsic transistor (Van der Ziel model) available in LIBRA, and by adding extrinsic elements (see Fig. 7) at room temperature T_a.

Fig. 8 shows the comparison between noise parameters obtained by our method and by measurement for two MESFET's of a MMIC foundry. These transistors have $0.5 \times 200\,\mu\text{m}^2$ and $0.5 \times 350\,\mu\text{m}^2$ gate dimensions, and are biased at $I_{\rm ds} = 0.6I_{\rm dss}$ and $I_{\rm ds} = 0.45I_{\rm dss}$ with $V_{\rm ds} = 5$ V. Good agreement between the predicted and measured values is obtained over the whole frequency range. The deviations observed are lower than 0.26 dB for the minimum noise figure value, 0.04 for the magnitude and 2.5° for the phase of the optimum reflection coefficient, and finally $2\,\Omega$ for the equivalent resistance value.

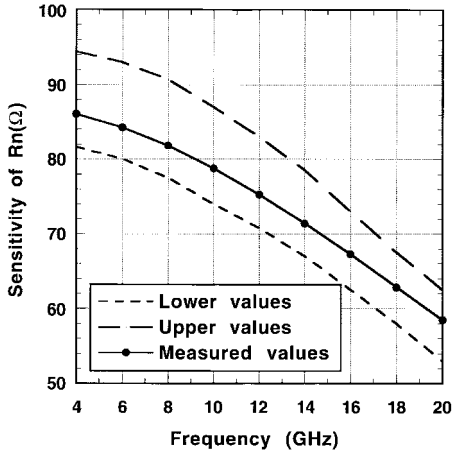


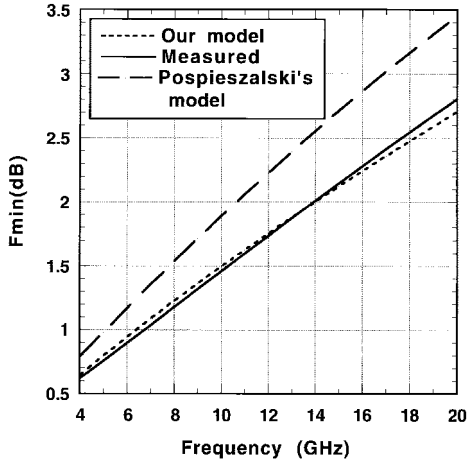
Fig. 9. Sensitivity of the noise resistance R_n to g_m uncertainties.

In addition, it can be concluded that all the approximations described in the preceding section are verified.

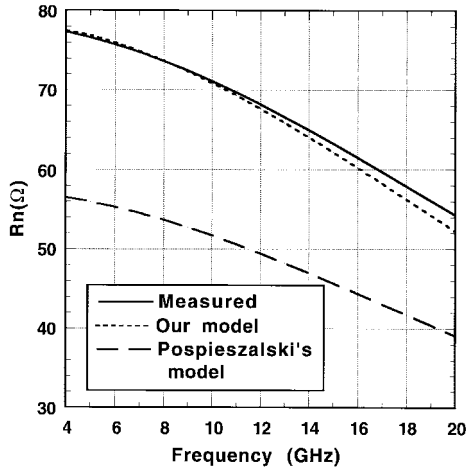
A simple study of the noise parameters sensitivity according to the extraction of the small signal equivalent circuit has been carried out for the $0.5 \times 200\,\mu\text{m}^2$ MESFET's gate dimension and biased at $I_{\text{ds}} = 0.6\,I_{\text{dss}}$. Supposing that the transconductance g_m is determined with an accuracy of 10% for the same MESFET at $I_{\text{ds}} = 0.2\,I_{\text{dss}}$ and at I_{dss}. The authors have obtained a noise coefficient P_1 that varies from 1.06 to 1.3 at $I_d = 0.2$ and a noise coefficient P_2 that varies from 2.67 to 3.26 at $I_d = 1$. By taking into account these variations, the accuracy of the MESFET noise parameters biased at $I_{\text{ds}} = 0.6\,I_{\text{dss}}$ is equal to $8\,\Omega$ for the noise resistance R_n (see Fig. 9), 0.35 dB for the minimum noise figure $F_{\min}$ at 20 GHz, 0.04 dB for the magnitude, and 2° for the phase of the optimum reflection coefficient. Generally, it is very difficult to make a better study of the sensitivity because the MESFET's elements are correlated. Therefore, the above example shows that the noise parameters obtained by the authors' method are not very sensitive to the elements of the equivalent circuit.

IV. Comparison with Other Methods

The authors demonstrate if it is possible to describe the transistors' noise parameters with the Pospieszalski model in [6] and [7]. Indeed by using (3) and [12, Eq. 12] for the intrinsic transistor, whose geometry is $0.5 \times 200\ \mu\text{m}^2$ and biased at $I_{\text{ds}} = I_{\text{dss}}/5$ and $V_{\text{ds}} = 5$ V. The authors have obtained that $\langle |e_h|^2 \rangle = 0.104$ $(\text{nV})^2/\text{Hz}$ and $\langle |i_h|^2 \rangle = 184$ $(\text{pA})^2/\text{Hz}$ in the 4–20-GHz frequency band. These correspond to temperature $T_d = 1540$ K for r_{ds} and $T_g = 250$ K for r_{gs}. By taking into account this result and knowing that resistances r_g, r_d, and r_s are at a temperature of 300 K, the authors have determined, thanks to the circuit shown in Fig. 2, the noise parameters of the MESFET according to the Pospieszalski model. Fig. 10 compares $F_{\min}$ and R_n of the MESFET using our model and the Pospieszalski model. The authors can see that the noise parameters obtained with the Pospieszalski model are in discrepancy with the measurements. The error on the noise resistance R_n is 20 Ω at 4 GHz (Fig. 10) and 0.75 dB on the minimum noise figure $F_{\min}$ at 20 GHz. This



(a)



(b)

Fig. 10. (a) The minimum noise figure and (b) the noise resistance of a $0.5{\times}200\,\mu\text{m}^2$ MESFET biased at $I_{\text{ds}} = I_{\text{dss}}/5$ and $V_{\text{ds}} = 5$ V.

discrepancy is due to the strong correlation (C_H) [12, Eq. (13)] between noise sources e_h and i_h (Fig. 11) that has been ignored in the Pospieszalski model. The same correlation phenomenon has been found by [18]. This correlation is due to the parasitic gate–source capacitance C_{gsp} which cannot be differentiated from the intrinsic capacitance C_{gsi} [18] and [19] by S-parameter measurement. In Fig. 2, the capacitance C_{gs} is equal to $C_{\text{gsi}} + C_{\text{gsp}}$.

Finally, since the Podell model [3] has been developed in the case where the noise sources are uncorrelated and is similar to that of the Pospieszalski and Gupta models, then this model cannot give with precision the noise parameters of the used MESFET's as a function of the gatewidth and bias current.

V. Conclusion

This paper presents a method that can be used to determine the noise parameters of transistors of the same technology with any dimension and any bias point. This method is based on the noise parameter measurement of a reference transistor T_r at two bias points. The authors have demonstrated it is possible to derive the noise parameters of any transistor T_i from two noise measurements of T_r and from the equivalent circuit of

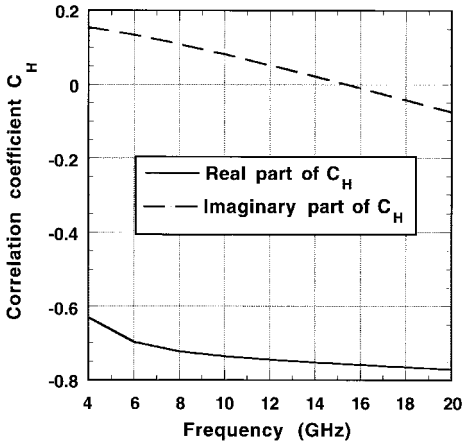


Fig. 11. The frequency dependence of the correlation coefficient of a MESFET biased at $I_{\rm ds} = I_{\rm dss}/5$ and $V_{\rm ds} = 5$ V.

transistor T_i. It should be noted that the dimensions of the transistors T_i and T_r are not necessarily equal. Finally, it is interesting to indicate that the noise model of the transistor is established from the Van der Ziel model, and can be used to study the noise behavior of MMIC circuits containing transistors at different bias points.

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